

FIG. 1

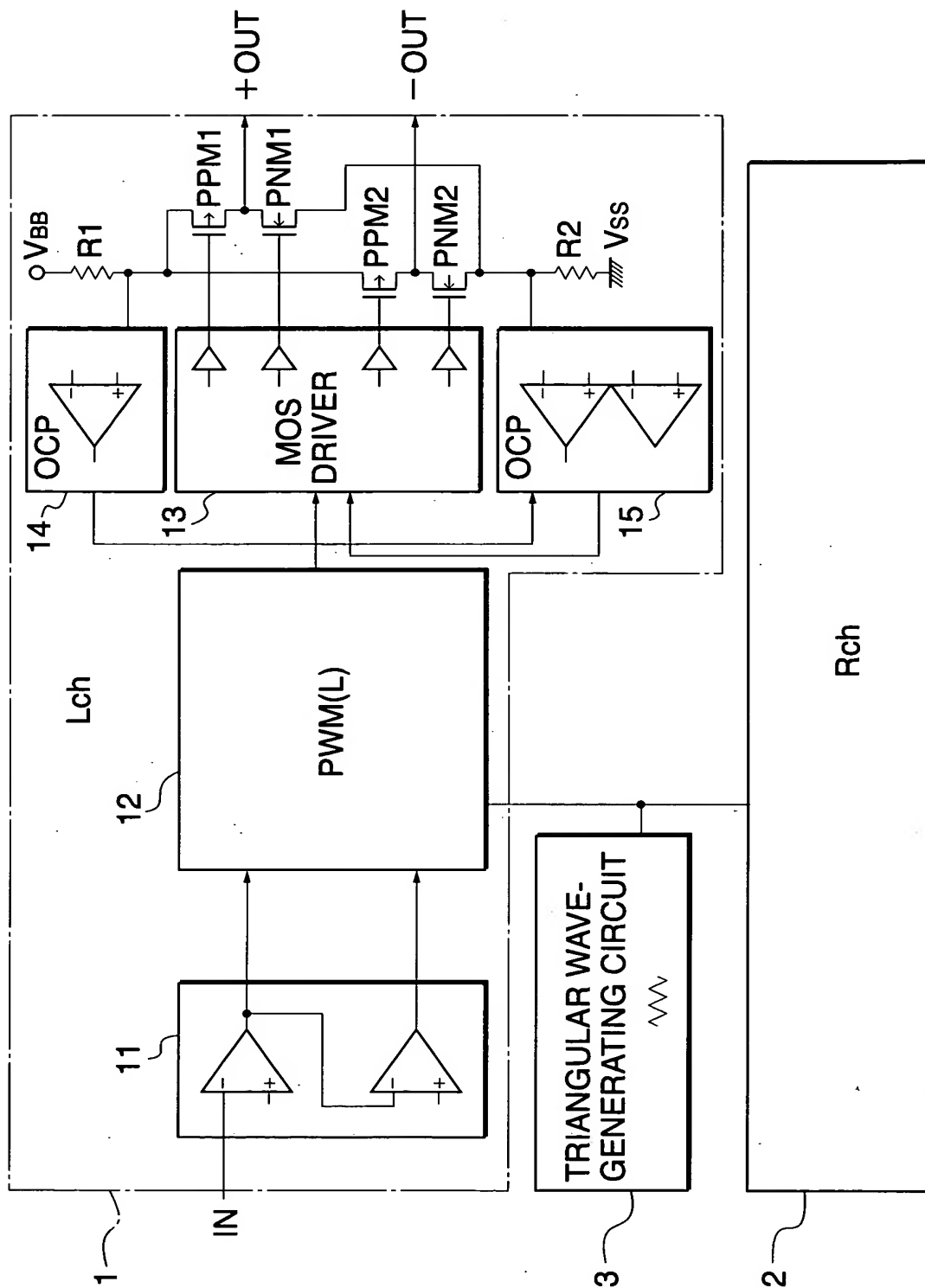
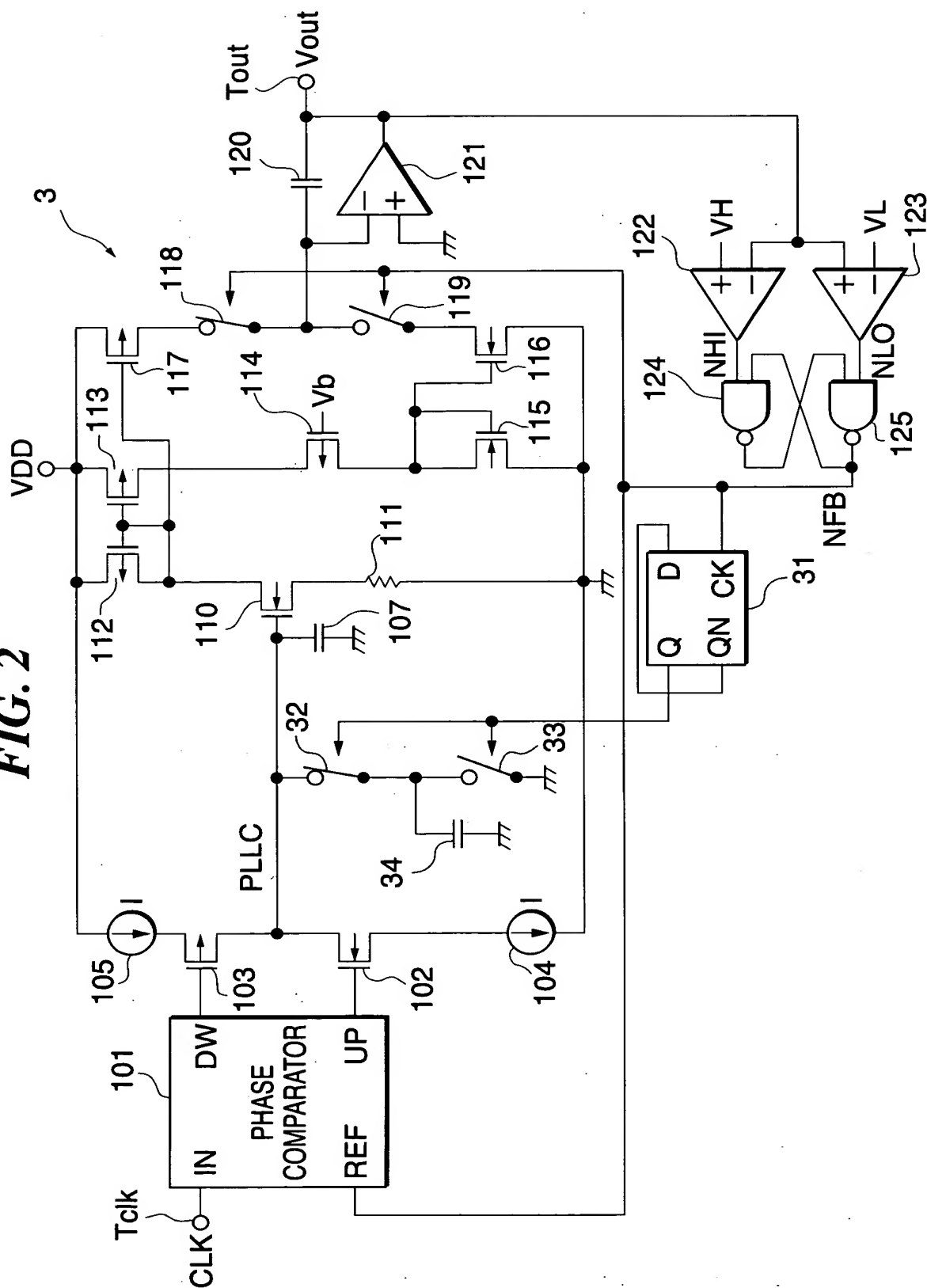


FIG. 2



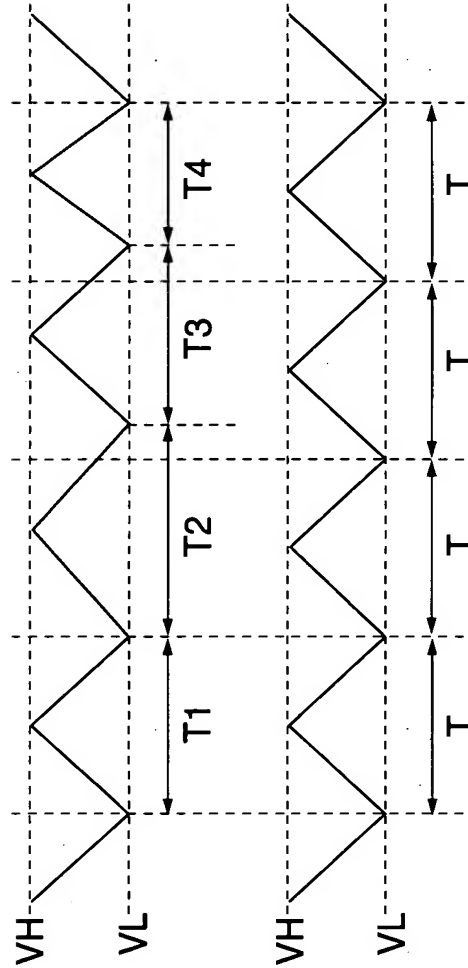


FIG. 3A

FIG. 3B

FIG. 4

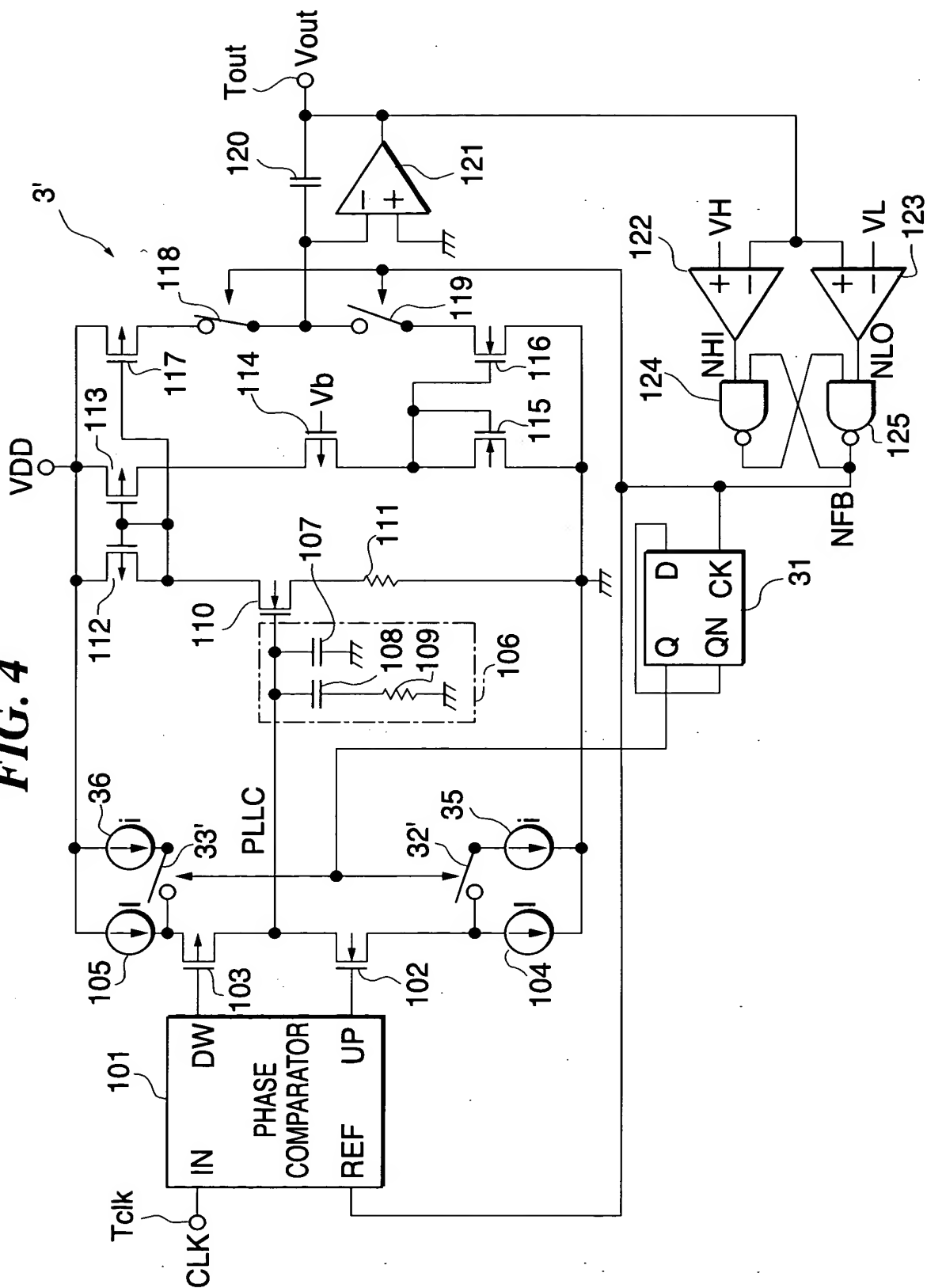
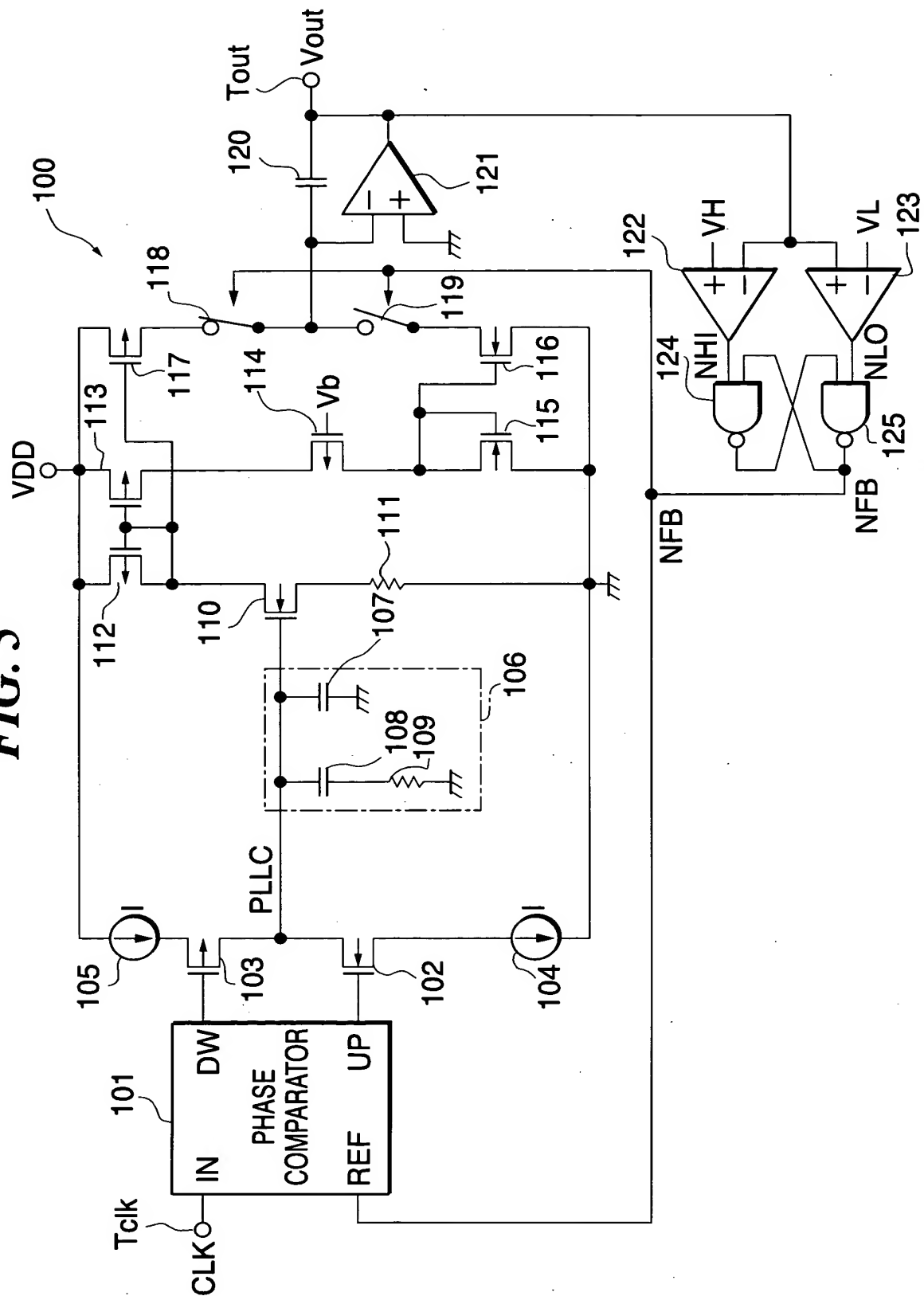


FIG. 5



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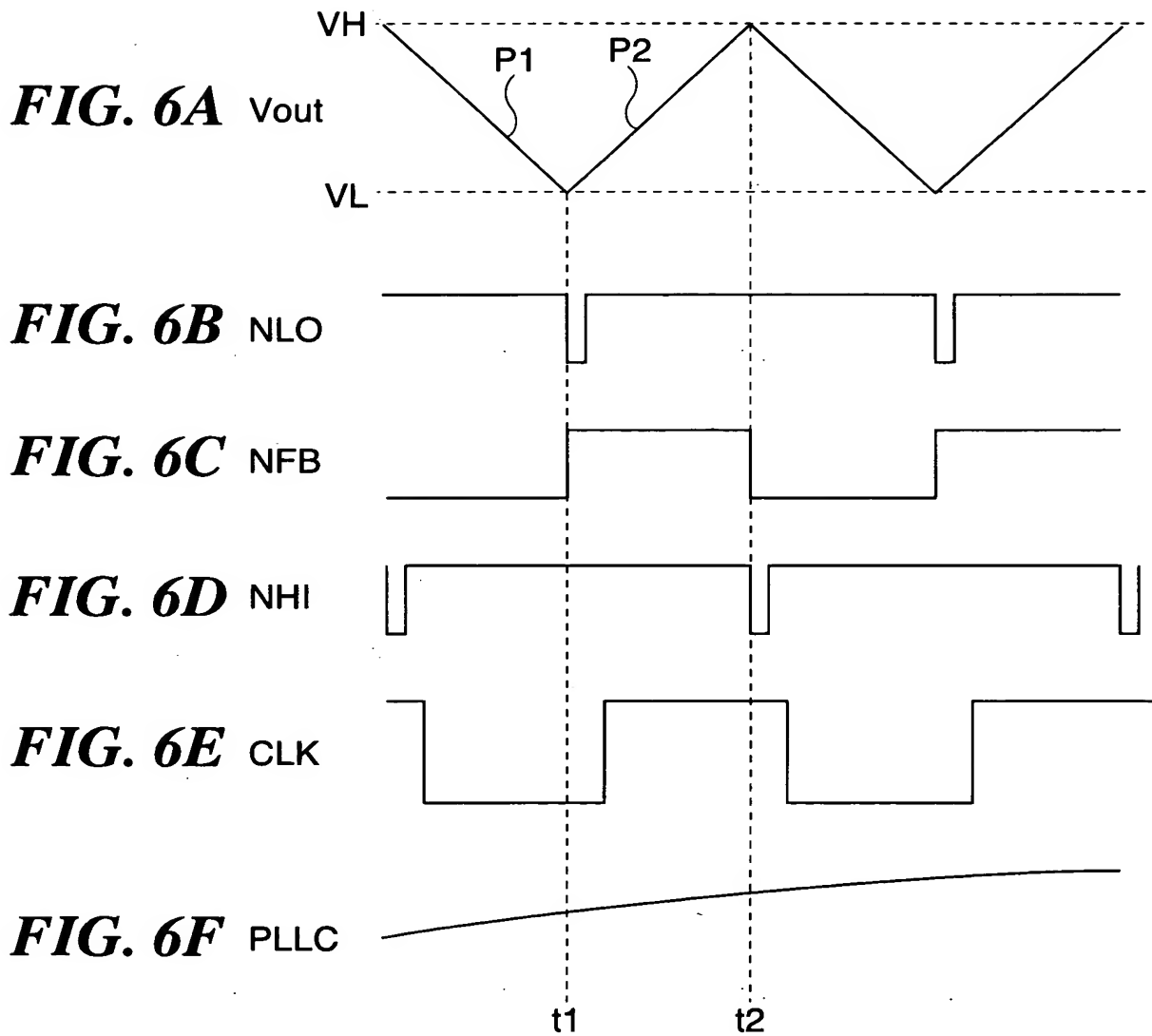


FIG. 8

The diagram illustrates a PLL system (5) with the following components and connections:

- Phase Comparator (101):** Receives **CLKO** at the **IN** input and **Tclk** at the **REF** input. It has control inputs **DW** and **UP**. Its output is connected to the **Q** input of a divider (31).
- Divider (31):** A counter/divider with inputs **Q**, **QN**, **CK**, and **D**. Its output is connected to the **NFB** input of the feedback loop.
- Feedback Loop:** Consists of a feedback divider (122) and two inverters (123, 124). The output of the divider is connected to the **NHI** input of inverter 123. The output of inverter 123 is connected to the **NLO** input of inverter 124. The output of inverter 124 is connected to the **NFB** input of the feedback divider. The output of inverter 123 is also connected to the **VH** input of the phase comparator.
- Charge Pump and Filter:** The output of the phase comparator is connected to the **PLL** input of a charge pump (102). The charge pump has two current sources (103, 104) and two output nodes (105, 106). The output of the charge pump is connected to the **Vb** input of the feedback divider.
- Output Stage:** The output of the feedback divider is connected to the **Tout** output of the system.

